Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs

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***Abstract*—The future of power conversion at low-to-medium voltages (around 650 V) poses a very interesting debate. At low voltages (below 100 V), the silicon (Si) MOSFET reigns supreme and at the higher end of the automotive medium-voltage application spectrum (approximately 1 kV and above) the SiC power MOSFET looks set to topple the dominance of the Si insulated-gate bipolar transistor (IGBT). At very high voltages (4.5 kV, 6.5 kV and above) used for grid applications, the press-pack thyristor remains undisputed for current source converters and the press-pack IGBTs for voltage source converters. However, around 650 V, there does not seem to be a clear choice with all the major device manufacturers releasing different technology variants ranging from SiC Trench MOSFETs, SiC Planar MOSFETs, cascode-driven WBG FETs, silicon NPT and Field-stop IGBTs, silicon super-junction MOSFETs, standard silicon MOSFETs, and enhancement mode GaN high electron mobility transistors (HEMTs). Each technology comes with its unique selling point with gallium nitride (GaN) being well known for ultrahigh speed and compact integration, SiC is well known for high temperature, electro-thermal ruggedness, and fast switching while silicon remains clearly dominant in cost and proven reliability. This article comparatively assesses the performance of some of these technologies, investigates their body diodes, discusses device reliability, and avalanche ruggedness.**

***Index Terms*—Body diode, cascode, reliability, silicon carbide (SiC) MOSFET, switching energy, wide bandgap devices.**

I. Introduction

SILICON technology has dominated power electronics for decades with silicon MOSFETs applied in high-frequency/low-power applications, silicon insulated-gate bipolar transistors (IGBTs) in medium-frequency/medium-power applications and silicon thyristors in high-power/low-frequency applications [1]. Because MOSFETs are unipolar devices, they are capable of fast switching since phenomena like tail currents and reverse recovery (due to stored charge from minority carriers) do not exist [2]. Hence, the switching rates are determined primarily by charging and discharging of parasitic capacitances, therefore, optimal MOSFET design that reduces these capacitances can enable high-frequency application. However, the unipolar nature means that conductivity modulation (enabled by carrier recombination) cannot be used to limit conduction losses. Hence, as the voltage level increases and thicker drift regions are required, MOSFETs demonstrate unacceptable conduction losses due to the increased ON-state resistance [2]. In low-voltage applications, like automotive systems that run off a 12 V battery, this is not a problem, however, as the voltage-level increases, the conduction losses suffered by MOSFETs make them inapplicable. Bipolar devices like IGBTs/BJTs and thyristors use drift and diffusion mechanisms for enabling current flow and conductivity modulation to reduce conduction losses [2]. Hence, these devices are more capable in automotive medium to higher voltage applications (600 V and above) like traction inverters for motor drives, wind/solar energy conversion systems in the case of IGBTs [3]. In ultrahigh power applications like current source converters for high-voltage direct current (HVdc) applications, the design and packaging of thyristors makes them the technology of choice [4].

The increased electrification of transportation, heat production, energy conversion, and other aspects of modern industry has increased demand for automotive medium voltage (around 650 V to 1 kV) power devices. This application space has historically been dominated by silicon IGBTs; however, this is changing. MOSFETs are applicable in automotive medium voltage applications only if the conduction losses are minimized by wide bandgap (WBG) materials like silicon carbide (SiC) [5] and gallium nitride (GaN) [6] or if innovative device design techniques like charge balance from super-junction layouts are used in silicon [7]. Hence, a plethora of 650 V to 1.2 kV SiC power MOSFETs have been commercialized alongside 600 to 900 V superjunction silicon MOSFETs and 650 V enhancement mode GaN FETs. For some time,

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only CREE (now Wolfspeed) and ROHM supplied SiC MOSFETs, however more companies like ST, Infineon, Littelfuse, and IXYS have released SiC MOSFETs. Fabricating these WBG MOSFETs is not trivial [8] since the most critical electrode (the gate) requires a reliable insulating metal/semiconductor interface with low interface and fixed oxide traps [9]. Developing reliable gate oxides in SiC has required a significant academic and industrial research effort [10]–[12] and yet it still lags silicon gate oxides while remaining completely illusive in GaN. As a result, non-MOSFET alternatives like JFETs [13], [14] and BJTs [15], [16] have been more widely explored using SiC and high electron mobility transistors (HEMTs) have been developed in the case of GaN [6]. Due to the lack of availability of bulk GaN substrates, GaN devices are typically lateral devices fabricated on foreign substrates (SiC, ceramic, and more recently silicon substrates) although vertical GaN devices have been investigated as research prototypes, however, with no commercial devices demonstrated [17].

Gate drivers in power electronics are well optimized for insulated gate transistors like MOSFETs and IGBTs, hence, these junction field effect transistors (JFETs)/bipolar junction transistors (BJTs) and depletion mode HEMTs have not been well received since there is significantly more power dissipated during the ON-state by the noninsulating gates [18]. Furthermore, these devices tend to be depletion mode meaning negative voltages are needed to turn them OFF. To solve these problems, SiC and GaN cascode configurations were developed. The cascode configuration comprises of a low-voltage silicon MOSFET driving a depletion mode GaN HEMT [19] or SiC JFET [20]. Hence, from the perspective of gate driving, these devices are comparable to silicon; however, the advantages of the WBG FETs are leveraged from the power side. These cascode devices have been released with 650 V ratings from United SiC (for SiC cascode) and Transphorm (for GaN Cascode), packaged in conventional TO-220 and TO-247 discrete packages. Other cascode options still at the research stage, including a low-voltage GaN HEMT driving a high-voltage SiC JFET, have been explored for very high switching frequencies (MHz) [21], [22].

Given the aforementioned advances in WBG technologies, silicon is not standing still. As far as cost and proven reliability is concerned, silicon remains undisputedly the best option. IGBTs have become faster with the latest generation of field-stop IGBTs competing favorably with FETs in terms of switching speed and conduction losses. The field-stop (punch-through) design uses an N+ buffer between the P+ collector and the N-drift region to significantly accelerate hole recombination during turn-OFF of the IGBT [3]. This vastly reduces the tail currents known to increase switching losses and limit switching frequencies in nonpunch-through IGBTs. Silicon superjunction MOSFETs are also capable of fast switching at 650 V. In applications where high reliability is demanded, silicon remains the technology of choice given the several decades of reliability and robustness data behind it. However, one disadvantage of IGBTs is the lack of a body diode, hence, antiparallel diodes are needed for reverse conduction capability.

As explained previously, the 650 V application space has become highly competitive. The purpose of this article is to highlight the benefits and drawbacks of each technology by comparative analysis. By measuring and characterizing some of the best in class technologies in the same circuits, we highlight their respective strengths and weaknesses. Table I shows important information (like current rating, voltage rating, packaging, die area, etc.) about the devices under test in this article.

TABLE I
POWER DEVICE TECHNOLOGY PARAMETERS

	SiC Cascode	SiC Trench	SiC Planar	Si CoolMOS™	Si IGBT
Voltage (V)	650	650	900	650	650
Current (A) (at 25°C)	31	39	36	43	40
Current (A) (at 100°C)	23	27	23	27	20
Die area (mm^2)	2.92	7.76	6.05	41.7	9.71
25°C R_{ON} (mΩ)	80	60	65	72	N/A
Packaging	TO-247	TO-247	TO-247	TO-247	TO-247
Cost (USD) 1 device	11.68	11.11	9.85	10.63	2.18
Cost (USD) 100 devices	946	862	963	797	148
Internal R_G (Ω)	4.5	12	4.7	0.75	N/A
Thermal Resistance (°C/W)	0.79	0.91	1	0.32	1

TABLE II
FIGURES OF MERIT

	SiC Cascode	SiC Trench	SiC Planar	CoolMOS™	Si IGBT
R_{SPEC} ($m\Omega.mm^2$)	233.6	465.6	393.3	3002.4	N/A
I density (A/mm^2)	10.6	5.02	6	1.03	4.1
Q_G (nC)	51 (400V)	58 (300V)	30.4 (400V)	161 (480V)	40 (300V)
R_{DSON}*Q_G (Ω.nC)	4.1	3.5	2	11.6	N/A

A good way to compare power devices from different technologies is to use figures-of-merit (FOM) that account for die area including specific-ON-state resistance (R_{SPEC}) and $R_{\mathrm{ON}} * Q_G$ (which accounts for the tradeoff between conduction and switching losses.) Table II shows the results of this comparison using values taken from datasheets. It can be seen from Table II that the SiC devices operate at higher current densities with the SiC Cascode JFET operating at approximately ten times the current density of the CoolMOS and twice the current density of the silicon IGBT. Furthermore, the R_{SPEC} of the SiC devices are one order of magnitude less than the CoolMOS device. Table II also shows that the $R_{\mathrm{ON}} * Q_G$ FOM for the SiC planar MOSFET is the best, followed by the Trench MOSFET and the Cascode JFET. The higher gate charge Q_G of the SiC cascode JFET is likely due to the low-voltage driving silicon MOSFET. However, because these parameters are often measured under different conditions, it is necessary to compare these devices under the same test conditions. This is what this article attempts.

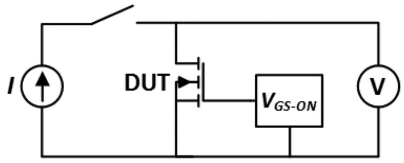

Fig. 1. Experimental test for conduction loss evaluation.

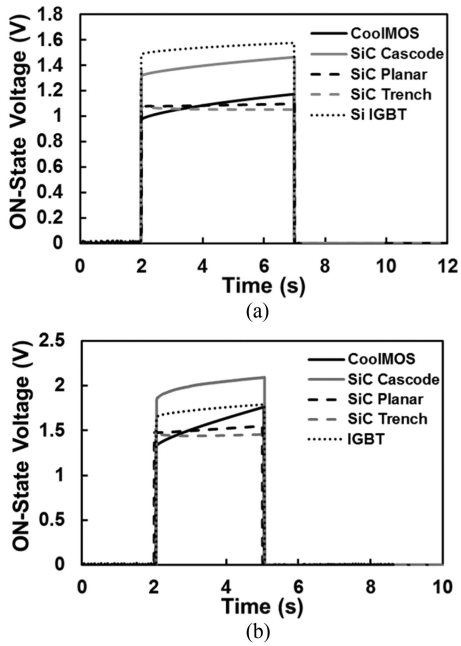

Fig. 2. v_{ON} versus time for the different technologies. (a) 15 A. (b) 20 A.

Section II looks at the conduction losses, Section III compares the switching losses, Section IV looks at body diodes while Section V compares the avalanche ruggedness, Section VI compares gate oxide reliability and Section VII concludes this article.

II. Conduction Performance

The conduction losses were measured by placing the device under test (DUT) in series with a current source with the DUT turned ON at its nominal gate voltage value. The DUT is placed on a heat sink and conducts current for a defined time, which is controlled by an auxiliary device similar to the dc power cycling [23]. The circuit is shown in Fig. 1. The measured ON-state voltage across the source drain is indicative of the conduction loss of the device and it was measured using a digital multimeter Hameg model HMC8012.

Fig. 2(a) shows the results of the measurements on the different technologies conducting a 15 A dc current for 5 s while Fig. 2(b) shows the case for 20 A dc current for 3 s. As the auxiliary device is turned ON and the current flows through the DUT, it is expected that the ON-state voltage will change over the duration that the device is conducting current. This is due to the temperature coefficient of the ON-state resistance, which in silicon MOSFETs increases as result of the reduced electron mobility at elevated junction temperatures. The rate of

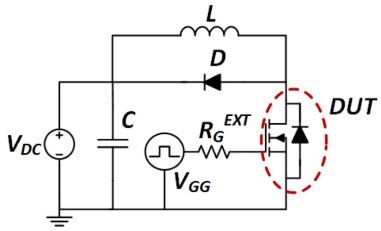

Fig. 3. Clamped Inductive Switching circuit for switching tests.

the change of the ON-state voltage with time is an indicator to the temperature coefficient of the conduction loss as well as the junction-to-case thermal impedance. All the devices are TO-247 packaged and the same external heat sink was used for these dc conduction tests. In this situation, the impact of the self-heating on the ON-state voltage will be determined by the transient junction-to-case thermal impedance of each device.

The results from Fig. 2(a) show that the SiC Trench MOSFET has the lowest conduction loss, followed by the SiC planar MOSFET, the CoolMOS device, the SiC Cascode, and then the silicon IGBT. The elimination of the JFET resistance in the trench design is critical for optimizing ON-state performance [24]. In Fig. 2(b), where the current is increased to 20 A, the SiC Trench MOSFET remains the best performing device followed by the SiC Planar MOSFET, the CoolMOS device, the silicon IGBT, and then the SiC cascode. The better performance of the IGBT compared to the SiC Cascode at 20 A is due to conductivity modulation, which makes the ON-state voltage less current dependent in IGBTs compared to MOSFETs [2].

It can also be observed from Fig. 2 that the temperature coefficient of the conduction loss in SiC is much lower than silicon since the ON-state voltage remains virtually flat over the 5 s that the device conducts current. The ON-state voltage rises with time in the SiC cascode because of high positive temperature coefficient of the SiC JFET. The Si IGBTs and CoolMOS devices show strongly positive temperature coefficients due to increased ON-state resistance with temperature in silicon devices [2].

One of the main advantages of SiC over silicon is the fact that it is more temperature invariant as can be seen from the measurements in Fig. 2. The losses are more stable over temperature. However, this makes condition monitoring in SiC more challenging since temperature sensitive electrical parameters have smaller temperature dependency [25].

III. Switching Performance

The switching performance of the devices have been tested using a standard clamped inductive double-pulse switching circuit shown in Fig. 3 where the low side device is the DUT and the high side diode D is a SiC Schottky diode. The transients were characterized using a double pulse and the turn-ON and turn-OFF switching energies have been measured for all the evaluated devices with five different gate resistances (R_G^{EXT}) at three different temperatures, for a load current of 20 A and a dc link voltage v_{dc} of 400 V. For high–temperature measurements, the device junction temperature was controlled using a controlled electric heater and thermal equilibrium between the device and

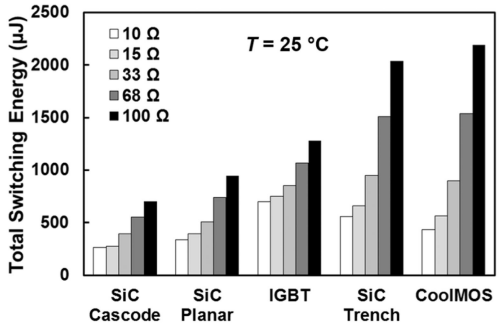

Fig. 4. Total switching energy for different gate resistances.

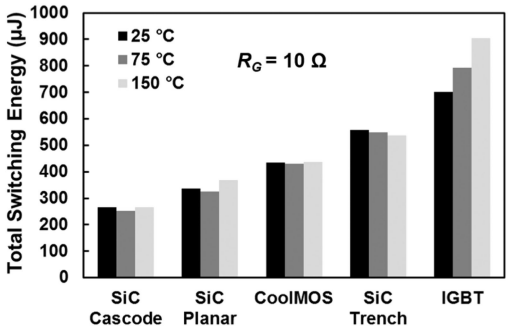

Fig. 5. Total switching energy for different junction temperatures.

the heater was ensured. The gate driver voltage V_{GG} used was the nominal gate driver voltage defined on the datasheets.

The measured switching losses at different gate resistances (R_G) are shown in Fig. 4, where it is observed that the SiC Cascode device followed by the SiC planar MOSFET performs best at all R_G. Depending on the R_G used, the order of performance changes. At $R_G = 10\ \Omega$ and $15\ \Omega$, the CoolMOS and trench MOSFETs perform better than the IGBT whereas at $R_G = 68\ \Omega$ and $100\ \Omega$, the IGBT performs better. The switching energies of the SiC Trench MOSFET and the CoolMOS device show significant dependence on the gate resistance most probably due to the higher and more nonlinear output capacitances. Fig. 5 shows the dependence of the switching energies on junction temperature with $R_G^{\mathrm{EXT}} = 10\ \Omega$.

In SiC MOSFETs, the turn-ON switching energy typically reduces with temperature due to the negative temperature coefficient of the threshold voltage [26]. Since the turn-OFF energy increases with temperature, the overall temperature coefficient of the switching energy is typically close to zero. In IGBTs, the formation of the carrier plasma in the drift region dominates the turn-ON switching rate, hence, turn-ON and turn-OFF switching energies increase with temperature due to the increase in carrier lifetime [26].

The turn-ON current switching rate (dI_{DS}/dt) and the turn-OFF voltage switching rate (dV_{DS}/dt) are indicators of the switching performance. Fig. 6(a) shows the turn-ON dI_{DS}/dt while Fig. 6(b) shows the turn-OFF dV_{DS}/dt for the different technologies switched with different gate resistances. The SiC cascode exhibits the highest current switching rates followed by the CoolMOS device, SiC planar device, the IGBT, and the SiC Trench MOSFET. In terms of turn-OFF switching rate, the SiC

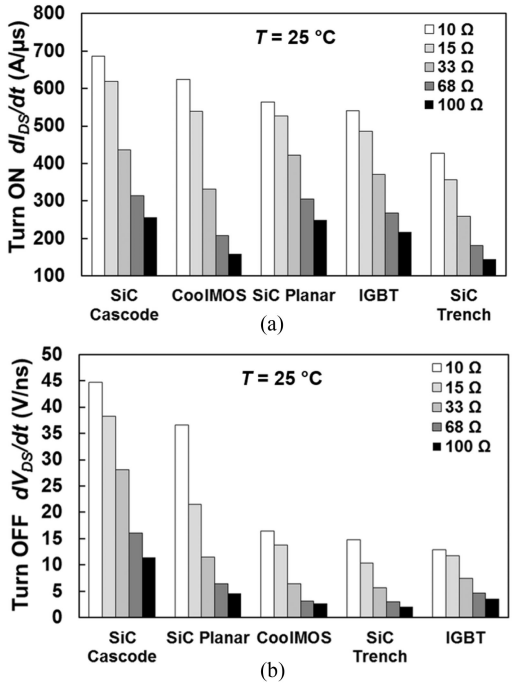

Fig. 6. (a) Turn-ON dI_{DS}/dt and (b) Turn-OFF dV_{DS}/dt for different technologies at different R_G^{EXT}.

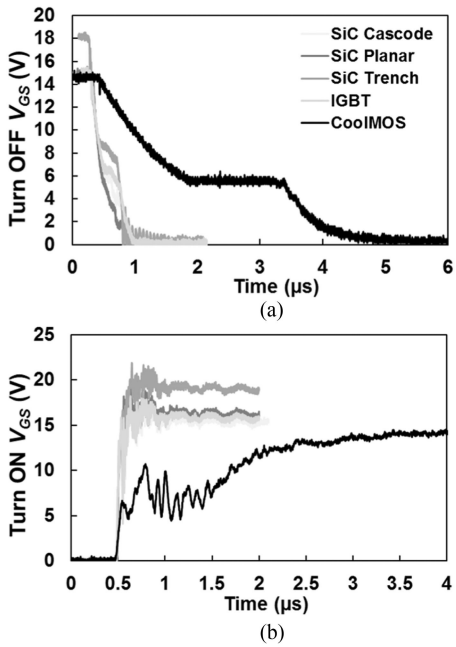

Fig. 7. Gate Voltage transient for all technologies at (a) turn-OFF and (b) turn-ON.

Cascode exhibits the highest dV_{DS}/dt, followed by the SiC Planar, the CoolMOS, the SiC Trench, and then the IGBT.

What is not clear from the results in Fig. 6, but is equally important, is the gate transient, which determines the maximum switching frequency the device can sustain. Fig. 7(a) shows the V_{GS} transient of all the devices during turn-OFF, where the CoolMOS device exhibits the longest transient. Fig. 7(b) shows the V_{GS} turn-ON transient where again, the CoolMOS ex-

TABLE III
PARASITIC CAPACITANCES

Device Technology	Input Capacitance (pF)	Output Capacitance (pF)
CoolMOS™	4400	754
SiC Planar	1500	100
SiC Trench	1000	126
SiC Cascode	1500	176
IGBT	1000	100

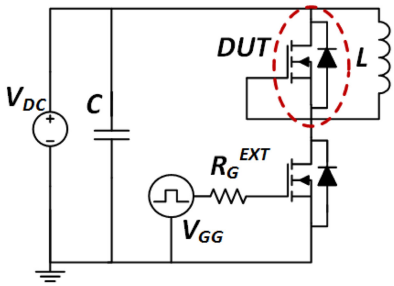

Fig. 8. Measurement circuit for body diode switching.

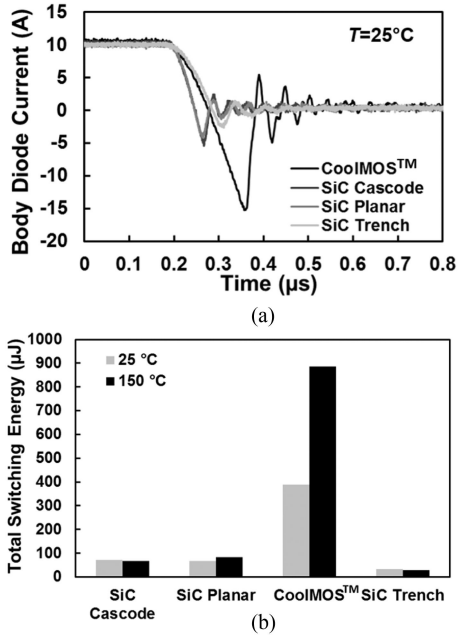

Fig. 9. (a) Reverse recovery characteristics of MOSFET body diodes in a leg configuration. (b) Switching energy of MOSFET body diodes.

hibits the longest transients. The gate resistance used was 100 Ω and the gate voltage used was the nominal V_{GS} defined by the manufacturer. Since the maximum switching frequency that the device can sustain is limited to the charging and discharging of the input and output capacitances, Fig. 7 shows the limitations of the CoolMOS device compared to the other devices. The reason for this significant disparity in the V_{GS} transient between the CoolMOS device and the remaining devices is the input and output capacitance. The values of the input and output capacitances, as shown in Table III.

IV. BODY DIODES

One important advantage MOSFETs have over IGBTs is the presence of a body diode [27], [28] that enables reverse conduction capability. The switching performance of the body diode has been measured using the circuit shown in Fig. 8, using a dc link voltage of 400 V.

By shorting the gate and the source of the high side transistor, it is removed from the circuit. The body diode of the MOSFET is a PiN diode since the low-doped N buffer acts as a charge storage region for minority hole carriers injected from the P+ body implant. Hence, the important power loss to consider is the turn-OFF loss since there is potential for reverse recovery, which is known to be a major contributor to losses in silicon PiN diodes.

When comparing the switching performance of the body diode of the different technologies, this can be done either by using the same technology on the low side and high side of the phase leg, which is representative of the application or by using the same low side transistor, which sets the same turn-OFF current rate (*dI/dt*) for all the high side diode. The first technique compares the actual performance of the body diode in the phase leg while the second technique sets the same conditions (turn-OFF *dI/dt*) for properly evaluating the reverse recovery of the body diode.

Fig. 9(a) shows the measured turn-OFF transients of all the body diodes. Since these measurements are performed using the same technology for high and low side device, the turn-OFF *dI/dt* imposed on the diodes are different. Fig. 9(b) shows the measured switching energies of the body diodes of the different technologies under these conditions. The results in Fig. 9(b) shows that the SiC body diodes exhibit the lowest switching energies. The very low minority carrier lifetime of holes in SiC means that there is very little stored charge in the body diode, hence, virtually no reverse recovery current. As a result, the reverse recovery performance of SiC PiN diodes shows near Schottky-like performance. The highest switching losses are exhibited by the CoolMOS device. It exhibits highest switching losses because of the superjunction design comprised of alternating P and N doped columns in the drift region of the device. This design causes additional stored charge in the body diode.

To make a fair comparison between the switching performances of the different body diodes, the measurements in Fig. 10 are repeated with the same low side transistor. This ensures that all the body diodes are subject to the same turn-OFF *dI/dt*. Fig. 10 shows the reverse recovery characteristics of the body diodes of the SiC Planar, SiC Trench, SiC Cascode, and CoolMOS devices, switched with the same bottom side device (SiC trench MOSFET, $V_{GS} = 15$ V and $R_G^{EXT} = 100\ \Omega$). In Fig. 10, opposed to Fig. 9(a), the switching rate of the bottom side device is the same and the reverse recovery characteristics are determined by the top-side body diode. The reverse recovery performance of the WBG body diodes is clearly superior to the CoolMOS body diode.

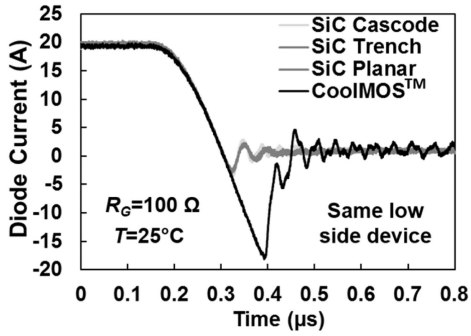

Fig. 10. Reverse recovery characteristics of MOSFET body diodes switched at the same rate.

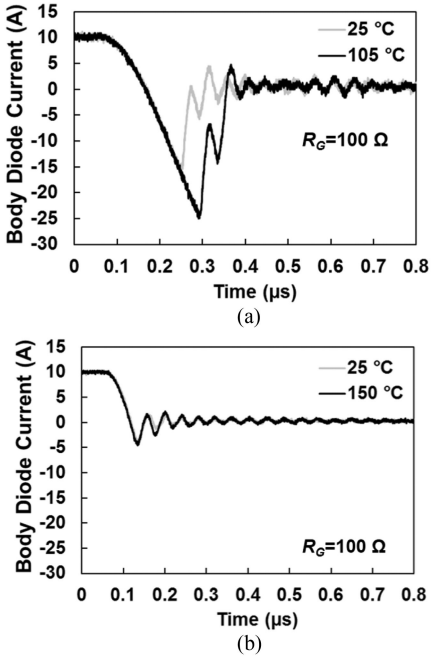

Fig. 11. Impact of temperature of reverse recovery of body diode. (a) CoolMOS. (b) SiC planar MOSFET.

As the junction temperature is increased, the switching energy of the CoolMOS body diode shows significant increase due to the positive temperature coefficient of the minority carrier lifetime, as shown in Fig. 11. Fig. 11(a) shows the reverse recovery characteristics of the CoolMOS body diode at 25 and 105 °C where the increase in peak reverse recovery current can be observed. In the SiC devices, the switching energy of the body diode is temperature invariant as the turn-OFF energy in Fig. 9(b) indicates and the turn-OFF transients of the diode current, measured at 25 and 150 °C, show in Fig. 11(b).

V. Avalanche Ruggedness

The ability of the power device to conduct current under unclamped inductive switching (UIS) is an indicator of the ruggedness of the device to electrical shocks [29], [30]. The device conducts avalanche current when current is forced through it (drain to source) with the channel OFF. The current causes

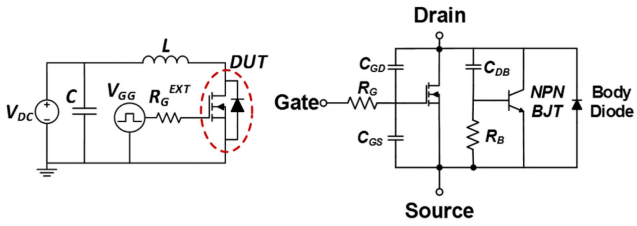

Fig. 12. Unclamped inductive switching circuit and MOSFET parasitics under UIS.

electron-hole generation through impact ionization, hence, the voltage across the device increases to its intrinsic breakdown voltage, which is usually higher than its rated voltage. Hence, there is significantly high instantaneous power dissipation within the device. The circuit for testing avalanche ruggedness is similar to Fig. 3 except that the clamping diode is removed, hence, it is called an unclamped inductive switching circuit. Fig. 12 shows the test setup together with a more detailed equivalent circuit of the power device where the parasitic capacitances are shown alongside the parasitic NPN BJT, and the p-body resistance R_B within the MOSFET. The failure mode under avalanche switching depends on the avalanche duration, which is set by the inductor in Fig. 12. If the inductor is small, then the avalanche current is high, and the avalanche duration is short. In this case, the failure mode is primarily determined by the latching of the parasitic NPN BJT shown in Fig. 12, followed by thermal hot spots from poor current sharing. Here, the heat is given insufficient time to diffuse across to the device to the case, hence, the thermal resistance of the device is not very important. On the other hand, if the inductor is large, then the avalanche duration is long, which means that the chip temperature rises more uniformly. In this case, the thermal resistance of the chip is important in determining the junction temperature.

The parasitic BJT can also latch under hard switching conditions particularly through the body diode. This occurs under high dV_{DS}/dt conditions when the internal capacitance within the drain-body (C_{DB}) produces a displacement current large enough to forward bias the emitter-base junction of the BJT assuming the voltage drop across the p-body resistance is large enough. Hence, this is more likely to occur under high-temperature conditions with fast switching.

Fig. 13 shows the UIS test pulses. As the DUT in Fig. 12 is pulsed with a high V_{GS}, current flows through it thereby charging the inductor at a rate of V_{dc}/L. During this phase, the V_{DS} is equal to the ON-state voltage. As the DUT is turned OFF, the inductor discharges the current stored in the magnetic field into the DUT, which raises its junction temperature as shown in Fig. 13. The maximum current and energy that the DUT can sustain before failure is determined by increasing the V_{GS} pulse length (and avalanche energy) progressively until the device fails. Fig. 14 shows the drain current through the device with different V_{GS} pulse lengths up to 360 μs where the device fails. Fig. 15 shows the corresponding V_{DS} waveforms during the UIS, where a sudden drop in V_{DS} is seen as the device fails at 360 μs pulse length. This has been done for all the technologies with 1 and 6 mH inductors to test both failure by parasitic BJT and failure by increased junction temperature from transient

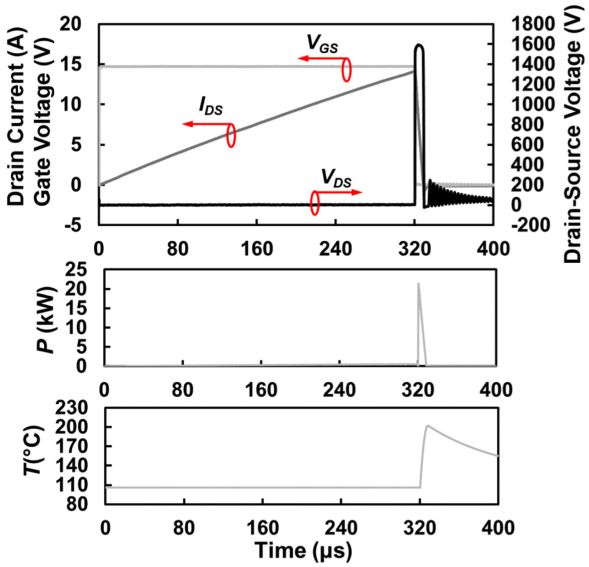

Fig. 13. V_{GS}, I_{DS}, V_{DS}, power, and junction temperature under UIS stress tests.

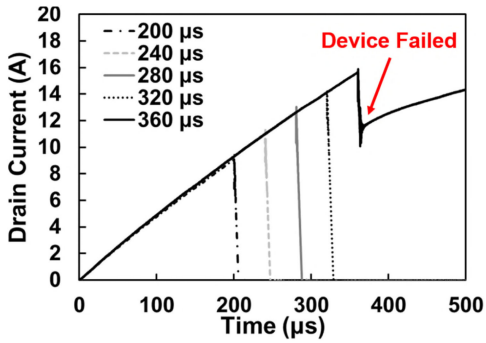

Fig. 14. Drain current through the DUT for different V_{GS} pulse lengths until device failure.

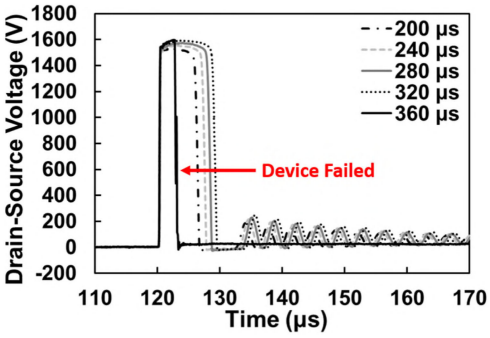

Fig. 15. V_{DS} voltage across the DUT for different V_{GS} pulse lengths until device failure.

thermal impedance. Devices of same type and two different current rating ranges (20 A at 25 °C and 40 A at 25 °C) were evaluated.

The results of the UIS tests on all the technologies are shown in Fig. 16 for the peak avalanche current at 25 °C and 105 °C. These tests were performed with the 1 mH inductor and were

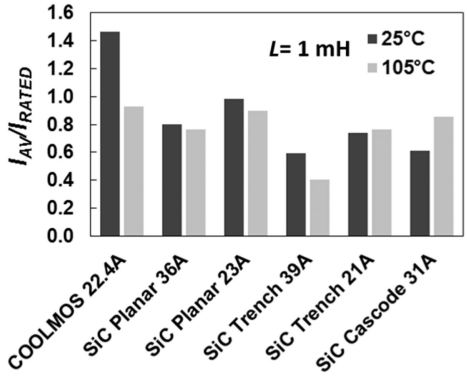

Fig. 16. Peak avalanche current ratio for different technologies with 1 mH inductor at 25 °C and 105 °C.

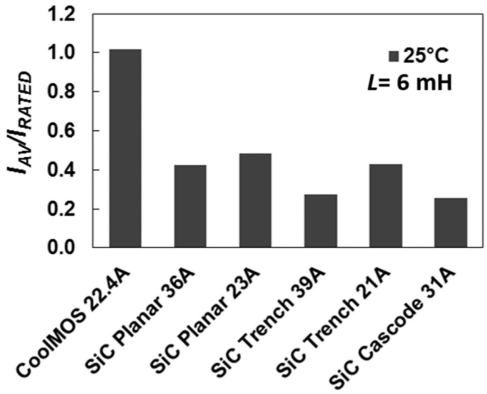

Fig. 17. Peak avalanche current ratio for different technologies with 6 mH inductor at 25 °C.

done of three devices to yield a statistical average. Fig. 17 shows the results of the UIS tests performed on the different technologies with the 6 mH inductor. Because the devices have different current ratings, the maximum avalanche current (before failure) has been normalized by the current rating. The results in Figs. 16 and 17 show that the CoolMOS device exhibits the highest avalanche current and energy at 25 °C.

However, as the junction temperature is increased to 105 °C, the performance of the CoolMOS device is not better than the SiC devices. Fig. 16 shows that the peak avalanche current of the CoolMOS device is more than twice that of the SiC devices when the inductor is increased to 6 mH. Of the remaining SiC devices, the Planar device exhibits the highest avalanche energy. The high performance of the CoolMOS in this situation is due to the lower thermal resistance, as shown in Table I.

Fig. 18 shows the peak avalanche energy dissipated by the different technologies using 1 and 6 mH inductors. It is clear from Fig. 18 that the devices dissipate more avalanche energy when the inductor is larger. This is because the avalanche duration is longer, hence, the entire chip is able to absorb all of the energy as opposed to a small section of it when a small inductor is used. The CoolMOS device is the best performing device under avalanche ruggedness for longer avalanche durations where the thermal impedance of the chip is critical for junction temperatures.

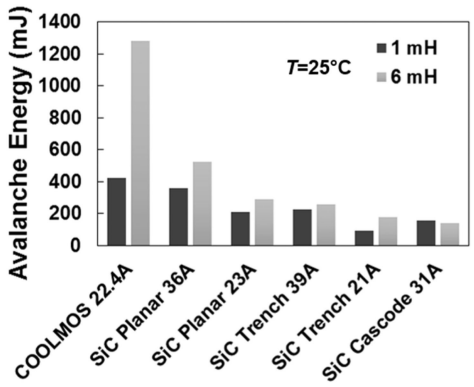

Fig. 18. Peak avalanche energy for different technologies 1 and 6 mH inductors.

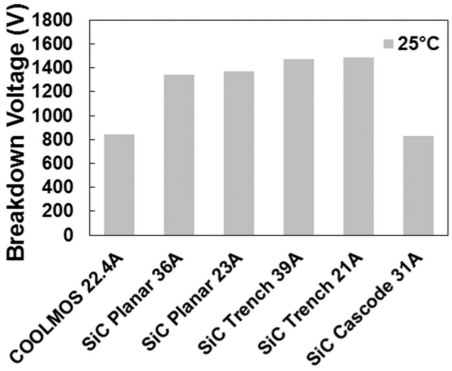

Fig. 19. Measured breakdown voltages during avalanche.

When the power device conducts current during UIS, the $V_{\rm DS}$ voltage is the actual breakdown voltage of the device. Fig. 19 shows the measured $V_{\rm DS}$ where the SiC Planar and Trench devices exhibit the highest breakdown voltages (approximately 1500 V) followed by the SiC Cascode and the CoolMOS devices. The actual breakdown voltages are important in applications where single event burn out from cosmic ray incidents have a higher probability of occurrence [31]. The SiC Planar and Trench devices are significantly de-rated (in voltage terms) compared to the CoolMOS and SiC cascode devices.

VI. Gate Oxide Reliability

As stated earlier, gate driving in power electronics is a critical component of device performance and ease of implementation [18]. Power electronics is based traditionally on normally OFF devices with good insulating interfaces for enabling low standby power. Silicon MOSFETs and IGBTs have done this for several decades with excellent reliability of the gate oxide. Because wide bandgap materials like SiC and GaN do not readily oxidize and form stable oxides with good insulating properties, the creation of a MOS interface has been challenging. In SiC, due to the presence of carbon atoms, thermal oxidation results in higher interface trap, and fixed oxide trap densities that cause threshold voltage instability, reduced breakover oxide voltage, and reduced time-dependent-dielectric-breakdown [10]–[12], [32].

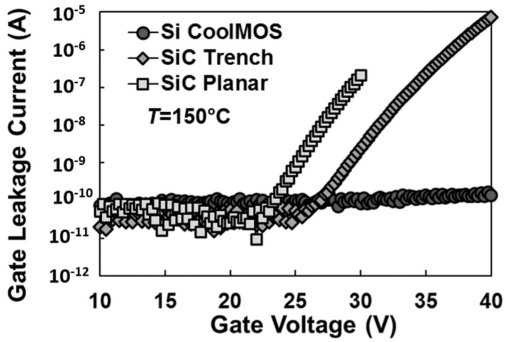

Fig. 20. Gate leakage current in MOSFET devices. $T = 150$ °C.

In GaN, thermal oxidation is not possible, hence, deposited gate dielectrics have been demonstrated in MIS-HEMTs [33].

Commercially available power devices are usually qualified as reliable if they pass a series of stress tests [34], [35] without exhibiting dielectric breakdown through high gate leakage currents, drain leakage currents, and threshold voltage shifts. The gate bias is usually positive, although negative gate bias tests are occasionally required for devices that are turned OFF with negative voltages. Threshold voltage shift due to gate voltage stress occurs due to charging of traps in the interface and in the oxide. When the $V_{\rm GS}$ stress is positive, upward shifts in $V_{\rm TH}$ occurs due to negative charge trapping and when the stress voltage is negative, downward shift in $V_{\rm TH}$ occurs due to the positive charge trapping. In silicon devices, these effects are well understood and have been suppressed with improved device fabrication processes. These effects are aggravated in SiC due to the increased trap density in the gate oxides [10], [12], [36]. Hence, it is well known that gate oxides are generally less reliable in SiC Planar and Trench MOSFETs although improvements have been made in the latest generation of devices [37], some of which are automotive qualified [38], [39]. An option to keep the ease-of-drive of silicon devices and the benefits of WBG power semiconductors is cascode design where a low-voltage silicon MOSFET is used in conjunction with a normally ON SiC JFET or GaN HEMT [19], [20].

Some simple tests have been performed in the SiC planar, Trench MOSFETs as well as the CoolMOS and IGBT devices. These include an oxide breakover voltage test where the gate voltage on the device is ramped up until the oxide conducts current. This is a quick indication of the strength of the oxide and how it will perform under $V_{\rm GS}$ stress testing. Fig. 20 shows the results where the CoolMOS device retains its oxide insulating properties with twice the rated voltage while the SiC Trench MOSFET and Planar MOSFETs experience oxide breakover at 28 and 24 V, respectively. Similar investigations have shown that gate oxides in silicon devices typically breakover at above 80 V [40].

Fig. 21 shows the gate transfer characteristics of the silicon IGBT before and after bias temperature instability (BTI) stress tests. The IGBT has been subjected to a stress voltage of 40 V for 1 h at a temperature of 150 °C (for positive BTI stress) and –40 V for 1 h at a temperature of 150 °C (for negative BTI stress). There was 16 h relaxation with $V_{\rm GS} = 0$ to allow for charge detrapping before the poststress gate transfer characteristics were

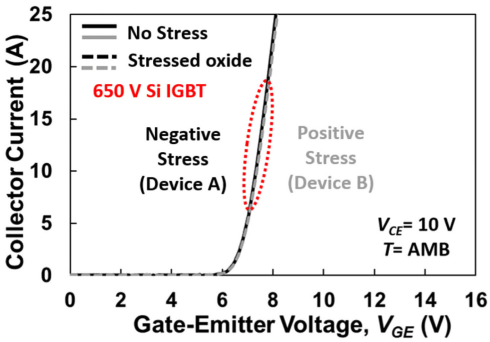

Fig. 21. Gate transfer characteristics for the silicon IGBT before and after NBTI and PBTI stress tests.

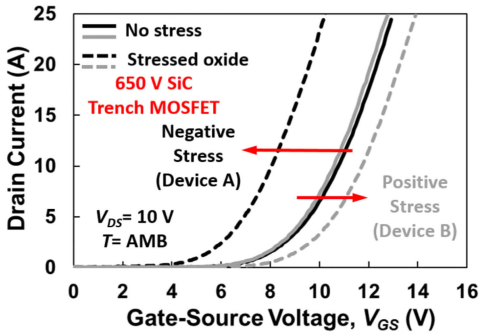

Fig. 22. Gate transfer characteristics for the SiC trench MOSFET before and after NBTI and PBTI stress tests.

measured. Under these conditions, only the permanent shift in V_{TH} is demonstrated since enough time has been allowed for the temporary shift to correct itself. Fig. 21 shows that the silicon IGBT is very reliable with no permanent shifts recorded.

Similar measurements using the same stress voltages and durations have been performed in the SiC Trench MOSFET with under PBTI and NBTI. The results in Fig. 22 shows a leftward shift for the device under NBTI stress indicating a reduction in the threshold voltage. Similarly, a rightward shift in the transfer characteristics is observable after PBTI stress thereby indicating an increase in the threshold voltage.

The measurements presented in Figs. 20, 21, and 22 have the objective of showing the differences between the gate reliability for both Si and SiC devices, using highly accelerated stress tests. Comparing the different commercially available SiC MOSFETs, studies have been performed in [10] and [40]. Without disclosing the manufacturers, different gate oxide reliability among commercially available SiC MOSFETs has been reported. Aichinger *et al.* [10] performed stresses at nominal gate voltage levels and captured the peak shift using a novel methodology for three different SiC MOSFETs (two trench and a planar). Different performances under BTI were reported, with a SiC trench MOSFET suffering high threshold voltage shifts and big dispersion among the number of devices tested. The other SiC trench MOSFET evaluated was the best performing, whereas, the planar SiC MOSFET had an intermediate performance.

Beier-Moebius and Lutz [40] tested different SiC MOSFETs under gate bias stress until failure, with completely different

TABLE IV
SUMMARY OF RESULTS

	SiC Cascode	SiC Trench	SiC Planar	Si CoolMOS™	Si IGBT
Conduction Loss	**	***	***	**	**
Specific ON-Resistance	***	**	**	*	*
Switching Loss	***	*	***	**	**
Body diode Switching	***	***	***	*	X
Gate Oxide Reliability	***	*	*	***	***
Avalanche energy	*	*	**	***	X
Cost	*	*	*	**	***

performance for the evaluated SiC MOSFETs, including devices breaking at voltages only 5 V higher than the nominal gate voltage and devices that required gate voltages stresses 40 V higher than the nominal voltage.

The results show that SiC MOSFETs still lag the silicon devices as far as gate oxide reliability is concerned.

VII. CONCLUSION

The automotive medium voltage market in power semiconductors is the most competitive market with a myriad of power devices available with different advantages and drawbacks. This article presented a comparative analysis of automotive medium voltage 650 V power devices including SiC Planar MOSFETs, SiC Trench MOSFETs, CoolMOS, SiC Cascode, and field stop IGBTs. The devices have comparable current ratings and are some of the best in class. Conduction losses, switching losses, body diode performance, avalanche ruggedness, and gate oxide reliability were studied.

As far the losses are concerned, the SiC Trench MOSFET is the best performing in conduction losses while the SiC Cascode device is best at switching with the SiC planar close behind. The CoolMOS device exhibits the highest capacitances because it is the largest chip as indicated by having the lowest thermal resistance. In terms of body diodes, the SiC devices are the best performing with very little switching energy followed by the SiC Cascode device with the silicon CoolMOS device exhibiting diode turn-OFF losses that can considerably high. The super-junction design of the CoolMOS device contributes to significant reverse recovery losses. However, in terms of avalanche ruggedness, the CoolMOS device is the best performing both for short and long avalanche durations although at higher junction temperatures, its performance is not better than SiC devices. As far as gate oxide reliability is concerned, silicon devices outperform SiC devices with much better performance under gate voltage stressing. In this sense, the SiC cascode device represented an excellent combination of SiC switching with silicon gate driving/reliability. This was because the input of the SiC Cascode JFET was a silicon MOSFET with typically excellent gate oxide reliability already established in silicon systems. However, as far as cost continues to remain a factor, the silicon IGBT is the most competitive device solution. Since silicon

IGBTs continue to remain competitive in terms of loss performance, the low cost and high reliability of the silicon IGBT mean it will continue to dominate for now. Table IV summarizes the findings in this article.

References

[1] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 2nd ed. Berlin, Germany: Springer-Verlag, 2018.

[2] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.

[3] B. J. Baliga, *The IGBT Device*. Amsterdam, The Netherlands: William Andrew, 2015.

[4] J. Przybilla, J. Dorn, R. Barthelmess, U. Kellner-Werdehausen, H. Schulze, and F. Niedernostheide, "Diodes and thyristor — Past, presence and future," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.

[5] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[6] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-Based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[7] B. Zhang, W. Zhang, M. Qiao, Z. Zhan, and Z. Li, "Concept and design of super junction devices," *J. Semicond.*, vol. 39, no. 2, Feb. 2018, Art. no. 021001.

[8] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[9] V. V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, "Intrinsic SiC/SiO_2 interface states," *Physica Status Solidi (a)*, vol. 162, no. 1, pp. 321–337, 1997.

[10] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliabil.*, vol. 80, pp. 68–78, 2018.

[11] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Understanding and modeling transient threshold voltage instabilities in SiC MOSFETs," in *Proc. IEEE Int. Reliabil. Phys. Symp.*, 2018, pp. 3B.5-1–3B.5-10.

[12] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of Threshold-Voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[13] A. Bhalla, X. Li, P. Alexandrov, and J. C. Dries, "The outlook for SiC vertical JFET technology," in *Proc. 1st IEEE Workshop Wide Bandgap Power Devices Appl.*, 2013, pp. 40–43.

[14] R. Siemieniec and U. Kirchner, "The 1200V direct-driven SiC JFET power switch," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[15] V. Niemela, A. Ravishunkar, and D. Kinzer, "SiC BJT minimizes losses in alternative energy applications," in *Proc. IEEE Energytech*, 2013, pp. 1–7.

[16] S. G. Sundaresan, A. Soe, S. Jeliazkov, and R. Singh, "Characterization of the stability of current gain and Avalanche-Mode operation of 4H-SiC BJTs," *IEEE Trans. Electron. Devices*, vol. 59, no. 10, pp. 2795–2802, Oct. 2012.

[17] S. Chowdhury and U. K. Mishra, "Lateral and vertical transistors using the AlGaN/GaN heterostructure," *IEEE Trans. Electron. Devices*, vol. 60, no. 10, pp. 3060–3066, Oct. 2013.

[18] D. Peftitsis and J. Rabkowski, "Gate and base drivers for silicon carbide power transistors: An overview," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7194–7213, Oct. 2016.

[19] F. Recht, Z. Huang, and Y. Wu, "Application note AN-0002 - characteristics of transphorm GaN power switches," 2016. [Online]. Available: https://www.transphormusa.com/en/document/characteristics-transphorm-gan-power-fets/: Transphorm

[20] Z. Li and A. Bhalla, "USCi SiC JFET cascode and super cascode technologies," in *PCIM AsiaInt. Exhib.Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2018, pp. 1–6.

[21] J. Xu, L. Gu, Z. Ye, S. Kargarrazi, and J. Rivas-Davila, "Cascode GaN/SiC power device for MHz switching," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2780–2785.

[22] J. Wei, H. Jiang, Q. Jiang, and K. J. Chen, "Proposal of a novel GaN/SiC hybrid FET (HyFET) with enhanced performance for high-voltage switching applications," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 99–102.

[23] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.

[24] T. Nakamura *et al.*, "High performance SiC trench devices with ultra-low ron," in *Proc. Int. Electron. Devices Meeting*, 2011, pp. 2651–2653.

[25] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. A. Mawby, "An investigation of Temperature-Sensitive electrical parameters for SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7954–7966, Oct. 2017.

[26] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An evaluation of silicon carbide unipolar technologies for electric vehicle Drive-Trains," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 517–528, Sep. 2014.

[27] S. Jahdi *et al.*, "An analysis of the switching performance and robustness of power MOSFETs body diodes: A technology evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2383–2394, May 2015.

[28] S. Tiwari, I. Abuishmais, J. K. Langelid, R. Lund, O. M. Midtgård, and T. M. Undeland, "Characterization of body diodes in the-State-of-the-Art SiC FETs-are they good enough as freewheeling diodes?" in *Proc. 20th Eur. Conf. Power Electron. Appl.*, 2018, pp. P1–P10.

[29] A. Fayyaz *et al.*, "A comprehensive study on the avalanche breakdown robustness of silicon carbide power MOSFETs," *Energies*, vol. 10, no. 4, pp. 1–15, 2017.

[30] P. Alexakis *et al.*, "Analysis of power device failure under avalanche mode Conduction," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, 2015, pp. 1833–1839.

[31] C. Felgemacher, S. V. Araújo, P. Zacharias, K. Nesemann, and A. Gruber, "Cosmic radiation ruggedness of Si and SiC power semiconductors," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 51–54.

[32] Z. Chbili *et al.*, "Modeling early breakdown failures of gate oxide in SiC power MOSFETs," *IEEE Trans. Electron. Devices*, vol. 63, no. 9, pp. 3605–3613, Sep. 2016.

[33] K. Geng, D. Chen, Q. Zhou, and H. Wang, "AlGaN/GaN MIS-HEMT with PECVD SiNx, SiON, SiO_2 as gate dielectric and passivation layer," *Electronics*, vol. 7, no. 12, pp. 1–11, 2018.

[34] S. Bahl, "Application-Relevant qualification of emerging semiconductor power devices," in *Proc. Presented Appl. Power Electron. Conf.*, Mar. 2016, [Online]. Available: http://www.ti.com/lit/wp/slyy091/slyy091.pdf

[35] N. Kaminski, "Reliability challenges for SiC power devices in systems and the impact on reliability testing," *Mater. Sci. Forum*, vol. 924, pp. 805–810, 2018.

[36] D. B. Habersat, A. J. Lelis, and R. Green, "Measurement considerations for evaluating BTI effects in SiC MOSFETs," *Microelectronics Reliab.*, vol. 81, pp. 121–126, 2018.

[37] R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs," *Japanese J. Appl. Phys.*, vol. 55, no. 4S, 2016, Art. no. 04EA03.

[38] Wolfspeed. E-Series Silicon Carbide MOSFETs and Diodes, 2019. [Online]. Available: https://www.wolfspeed.com/e-series

[39] Rohm. ROHM Now Offers the Industry's Largest Lineup of Automotive-Grade SiC MOSFETs, 2019. [Online]. Available: https://www.rohm.com/news-detail?news-title=industrys-largest-lineup-of-automotive-grade-sic-mosfets&defaultGroupId=false

[40] M. Beier-Moebius and J. Lutz, "Breakdown of gate oxide of SiC-MOSFETs and Si-IGBTs under high temperature and high gate voltage," in *Proc. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2017, pp. 1–8.

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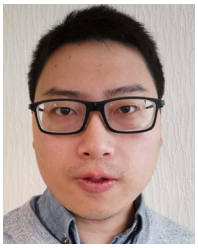

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